Test and Measurement
Division

Operating Manual

Option: Digital Baseband Interface

R&S® FSQ-B17

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Dear Customer,

Contents

Caution* regarding the use of the instrument with the R&S FSQ-B17 option installed*:

The instrument complies with the emission requirements stipulated by EN 55011 class A. This means that the instrument is suitable for use in industrial environments. In accordance with EN 61000-6-4, operation is not covered in residential, commercial, business areas nor in small-size companies.

The instrument must not be operated in residential, commercial, business areas or in small-size companies, unless additional measures are taken so that EN 61000-6-3 is met.

General Description

For evaluation of IQ data, the R&S FSQ in standard configuration provides internal IQ memory for capturing IQ data, which can be output via GPIB or the LAN interface. The optional digital baseband interface (R&S FSQ-B17) provides an online IQ data output on the rear panel of the R&S FSQ.
The output of online data via the IQ data interface is configured via remote control.
Fig. 4-21 shows the location of the IQ interface in the digital signal processing chain.

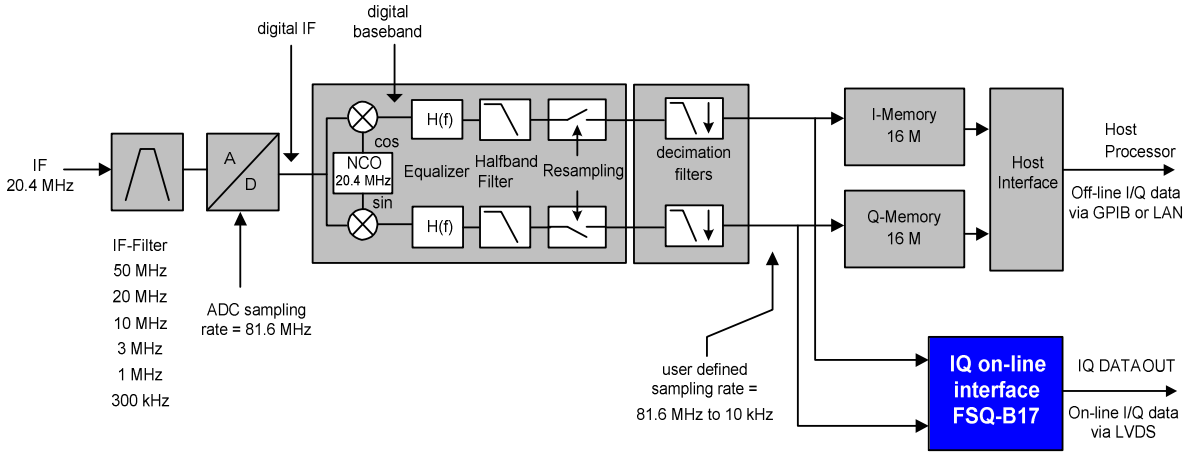


Fig. 1 Block diagram of the IQ downconverter

The RF input signal is down-converted to a fixed IF frequency of 20.4 MHz. The IF signal is digitized using an A/D converter with 81.6 MHz sampling rate. An analog bandpass filter in front of the A/D converter limits the spectrum (bandwidth is user-selectable).
The digital IF is down-converted to the IQ baseband using a digital mixer fed by a numerical controlled oscillator (NCO). Before further processing, a digital equalizer filter corrects the amplitude and phase distortion of the analog signal path of the R&S FSQ.
The output sampling rate can be adapted to the actual signal bandwidth by means of downsampling. This is done by a resampler which reduces the sampling rate from 81.6 MHz to 40.8 MHz, followed by a 2^{-n} decimation (with n = 0 to 12); the reduction of the sampling rate is continuously programmable. Finally, the output sampling rate can be adjusted from 81.6 MHz to 10 kHz. Prior to downsampling in the resampler and the decimation filter block, the I/Q signal is filtered by low pass filters in order to avoid aliasing products due to the decimation.

As long as there is no trigger signal, the I/Q data is written continuously into the IQ memory and in parallel is accessible online at the I/Q interface R&S FSQ-B17. The word length of the data is 20 bits fixed point for each I and Q.

In order to get an uninterrupted data stream when using the R&S FSQ-B17 online interface , the trigger mode must be set to EXTERNAL and no trigger signal must be applied to the EXT TRIGGER input at the same time.

Note: *With the trigger mode set to EXTERNAL, the instrument waits for a trigger signal while the data acquisition is running in an endless loop. As any trigger event would stop the data acquisition, no signal may be connected to the EXT TRIGGER input. Trigger mode IMMEDIATE (free run) is also not appropriate, as it does not provide data acquisition in an endless loop, which is required for a continuous data stream.*

Depending on the sample rate, the following bandwidths are available:

Sample rate (from)	Sample rate (to)	Max. bandwidth
81.6 MHz	40.8 MHz	30 MHz
40.8 MHz	20.4 MHz	0.68 sampling rate
20.4 MHz	10 kHz	0.8 sampling rate

The selected IF bandwidth (RBW setting) limits the equalized bandwidth as follows:

RBW	Equalized band-width
<3 MHz	not equalized
3 MHz	2 MHz
5 MHz	3 MHz
10 MHz	7 MHz
20 MHz	17 MHz
50 MHz	28 MHz

Online Interface

The online interface is an LVDS interface, compatible with LVDS channel link introduced by National Semiconductor (please refer to http://www.national.com/appinfo/lvds/files/channellink_design_guide.pdf for additional information).

Compatible receiver and deserializer: DS90CR486 (also suitable: DS90CR484)
(data sheet available at: http://www.national.com/ds/DS/DS90CR486.pdf)

Fig. 2 below shows a general overview of the IQ data interface.

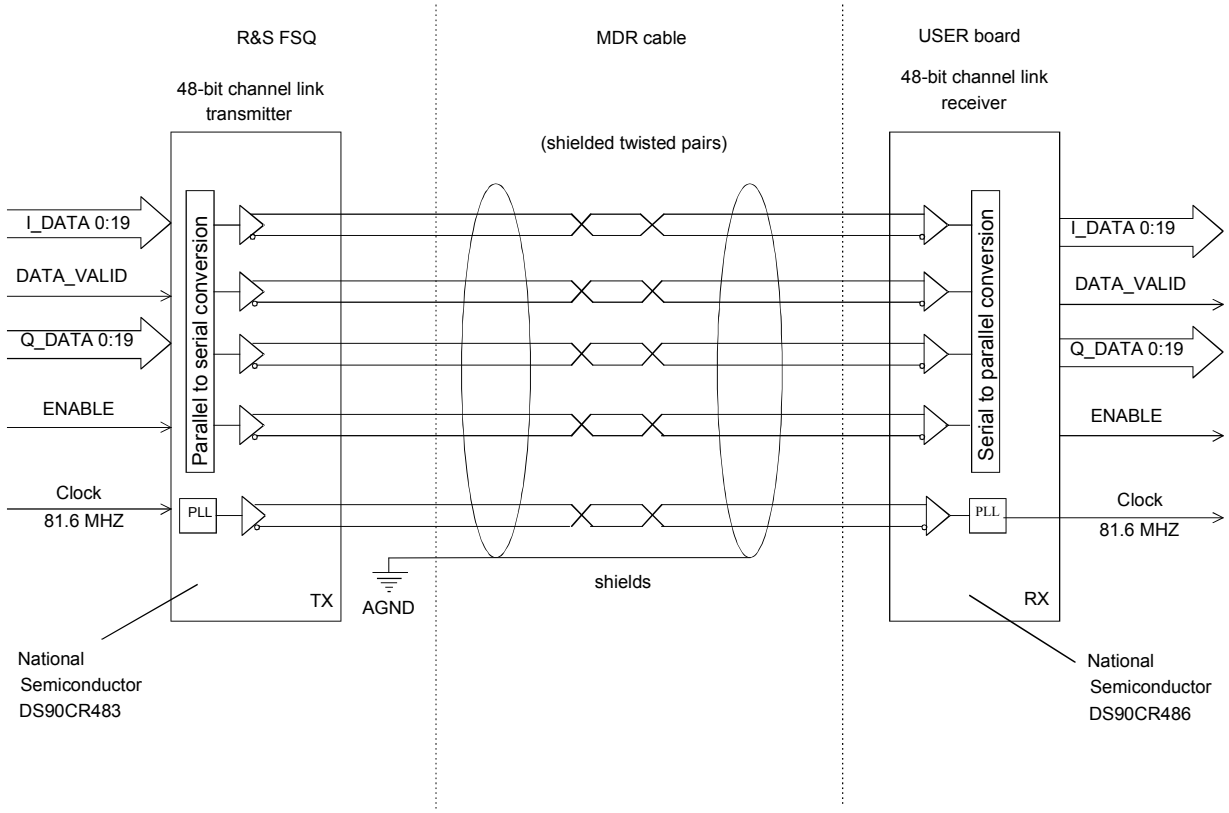


Fig. 2 R&S FSQ LVDS interface connection overview

Fig. 3 shows the functional timing diagram of the interface.

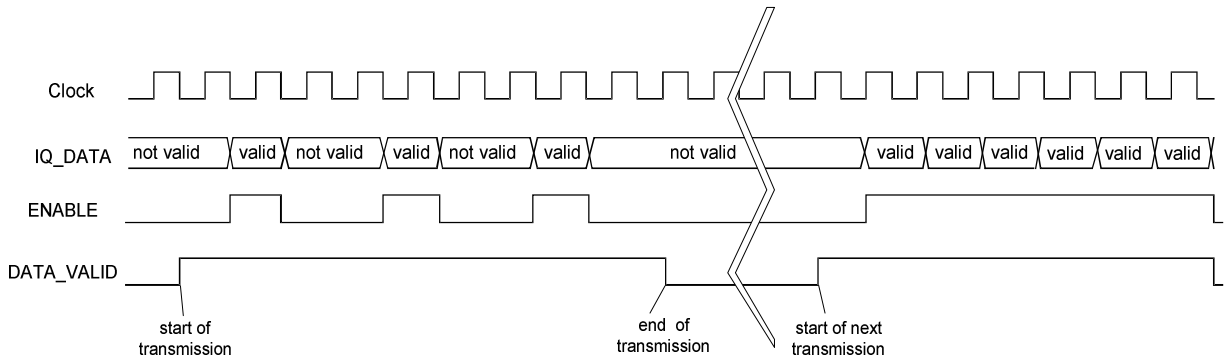


Fig. 3 Functional timing diagram

Signal Description

Clock: Sample clock from the R&S FSQ with a frequency of 81.6 MHz. It writes the parallel IQ data into the channel link transmitter with the positive edge. The user application must read the transmitted data out of the channel link receiver also with the positive edge of this signal.

I_DATA0:19: Real data 20 bits

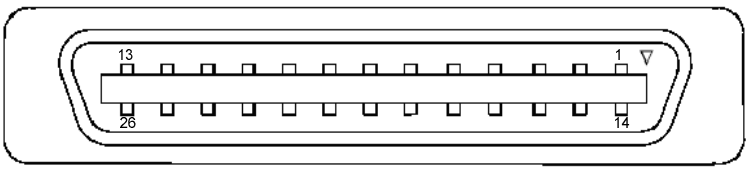
Q_DATA0:19: Imaginary data 20 bits

ENABLE: Signals the validity of individual data during a data transmission.
Note:
The user-defined sampling rate can be lower than the fixed 81.6 MHz data rate of the interface. When the sampling rate is lower than 81.6 MHz, not all transmitted data are valid samples. The ENABLE bit in state "high" indicates the valid samples.

DATA_VALID: Defines the start and stop event of the data transmission. The transmission starts on the rising edge of DATA_VALID and stops on the falling edge. Data are only valid while DATA_VALID is "high".

Signal Assignment

Connector



Connector on R&S FSQ rear panel, connector front view.

Connector type: 26 pin female 0.050" Mini D Ribbon connector (e.g.: 3M 102XX-1210VE series)

Pin description:

This table shows the multiplexed data at the output of the LVDS transmitter.
(DS90CR483 is used as transmitter. For further information on multiplexing/demultiplexing scheme, please refer to http://www.national.com/ds.cgi/DS/DS90CR483.pdf)

Pin	Signal	Level	
1			reserved for future use
2	GND	0V	Ground, shield of pair 1-14, for future use
3	SDAT0_P	LVDS	Serial data channel 0 positive pin; carries the bits VALID, ENABLE, MARKER_1, Reserve_1, RE_0, RE_1
4	SDAT1_P	LVDS	Serial data channel 1 positive pin; carries the bits RE_2, RE_3, RE_4, RE_5, RE_6, RE_7
5	SDAT2_P	LVDS	Serial data channel 2 positive pin; carries the bits RE_8, RE_9, RE_10, RE_11, RE_12, RE_13
6	CLK1_P	LVDS	Clock 1 positive pin; clock for transmission on LVDS link
7	S_CLK	TTL	(for future use)
8	+5VD	+5.0V	Supply voltage (for future use)
9	SDAT3_P	LVDS	Serial data channel 3 positive pin; carries the bits RE_14, RE_15, RE_16, RE_17, RE_18, RE_19
10	SDAT4_P	LVDS	Serial data channel 4 positive pin; carries the bits TRIGGER_1, TRIGGER_2, MARKER_2, Reserve_2, IM_0, IM_1
11	SDAT5_P	LVDS	Serial data channel 5 positive pin; carries the bits IM_2, IM_3, IM_4, IM_5, IM_6, IM_7
12	SDAT6_P	LVDS	Serial data channel 6 positive pin; carries the bits IM_8, IM_9, IM_10, IM_11, IM_12, IM_13
	SDAT7_P	LVDS	Serial data channel 7 positive pin; carries the bits IM_14, IM_15, IM_16, IM_17, IM_18, IM_19
14			reserved for future use
15	SDAT0_M	LVDS	Serial data channel 0 negative pin
16	SDAT1_M	LVDS	Serial data channel 1 negative pin
17	SDAT2_M	LVDS	Serial data channel 2 negative pin
18	CLK1_M	LVDS	Clock 1 negative pin
19	DGND	0V	Power ground; ground return for 5V supply voltage (for future use)
20	S_DATA	TTL	(for future use)
21	SDAT3_M	LVDS	Serial data channel 3 negative pin
22	SDAT4_M	LVDS	Serial data channel 4 negative pin
23	SDAT5_M	LVDS	Serial data channel 5 negative pin
24	SDAT6_M	LVDS	Serial data channel 6 negative pin
25	SDAT7_M	LVDS	Serial data channel 7 negative pin
26	GND	0V	LVDS ground; shielding of transmission lines and shielding of cable

Channel Link Receiver

This table shows the demultiplexed data at LVDS receiver output. (Recommended receiver: DS90CR486 or DS90CR484). For further information on multiplexing/demultiplexing scheme, please refer to http://www.national.com/ds/DS/DS90CR486.pdf

Data bit	Signal name	
D47	IM_19	Imaginary part, bit 19, Q signal (MSB)
D46	IM_18	Imaginary part, bit 18, Q signal
D45	IM_17	Imaginary part, bit 17, Q signal
…		
D29	IM_1	Imaginary part, bit 1, Q signal
D28	IM_0	Imaginary part, bit 0, Q signal (LSB)
D27	Reserve_2	reserved for future use
D26	MARKER_2	Marker bit 2, e.g. marking of beginning or end of a burst (high = active / low = inactive)
D25	TRIGGER_2	Trigger bit 2, marking of trigger event (high = active / low = inactive)
D24	TRIGGER_1	Trigger bit 1, marking of trigger event (high = active / low = inactive)
D23	RE_19	Real part, bit 19, I signal (MSB)
D22	RE_18	Real part, bit 18, I signal
D21	RE_17	Real part, bit 17, I signal
…		
D5	RE_1	Real part, bit 1, I signal
D4	RE_0	Real part, bit 0, I signal (LSB)
D3	Reserve_1	reserved for future use
D2	MARKER_1	Marker bit 1, e.g. marking of beginning or end of a burst (high = active / low = inactive)
D1	ENABLE *	Indicates valid data word (high = valid, low = invalid)
D0	VALID *	Indicates valid data transmission (high = valid, low = invalid)

* The data rate is always 81.6 MHz. The sampling rate can be set from 10 kHz to 81.6 MHz. When the sampling rate is lower than 81.6 MHz, not all transmitted data are valid samples. The ENABLE bit indicates the valid samples. The VALID bit is high during the entire data transmission.

D47 to D28: one 20-bit-wide sample, imaginary part
D23 to D4 : one 20-bit-wide sample, real part
D27 to D24, D3 to D0: control bits for data transmission

Cable

The cable configuration (twisted pairs, shielding) must match the signal assignment.
The LVDS transmission lines must be twisted pairs with a characteristic impedance of 100 ± 10 ohms, each pair individually shielded.
Conductor size of the additional wires: AWG28
Connectors on cable: 26 pin male 0.050" Mini D Ribbon plug (e.g.: 3M 103XX-3210 Series)
Maximum cable length: 2 m (e.g.: 3M 14526-EZHB-200-0QC cable with 200 cm length)

Remote Operation

The R&S FSQ is operated as a receiver (zero span). The instrument is tuned to the signal to be measured by setting the center frequency and the reference level. For best performance, the reference level should be set slightly higher than or equal to the expected peak power of the signal.

The digital down conversion and the online interface (R&S FSQ-B17) are controlled by the Trace:IQ subsystem (for additional information, please refer to R&S FSQ operating manual, volume 2, TRACe:IQ subsystem).

Analyzing an RF signal

Programming example

The following signal has to be measured:

carrier frequency	5 GHz
peak power	-10 dBm
bandwidth	22 MHz

The wanted sampling rate is 36 MHz

Depending on the signal bandwidth, the IF bandwidth (RBW) = 50 MHz must be chosen.

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*RST                                  / sets the instrument to a defined default status
INST:SEL SAN                          / selects the operating mode spectrum analyzer
FREQ:CENT 5GHz                        / sets the center frequency to 5 GHz
FREQ:SPAN 0                           / set the span = zero
DISP:TRAC1:Y:RLEV -10dBm              / sets the reference level to -10 dBm
TRAC:IQ:SET NORM,50MHz,36MHz,EXT,POS,0,1000   / configures the measurement *)
                                        Filter type: Normal
                                        RBW: 50 MHz
                                        Sample Rate: 36 MHz
                                        Trigger Source: External
                                        Trigger Slope: Positive
                                        Pretrigger Samples: 0
                                        # of Samples: 1000
TRACE:IQ:STATE ON                     / enables acquisition of I/Q data
OUTPUT:DIQ ON                         / enables digital I/Q data output interface
INPUT:SELECT RF                       / selects the RF input as signal input
INIT:IMM                              / starts data acquisition and transmission
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*) Only the settings of RBW, sample rate and trigger source EXT are relevant to the digital baseband interface. The other parameters can be set as shown as default.